PRAKLA-SEISMOS INFORMATION No.15

Array Processor System APS

Contents

Introduction

The most important component of the seismic system SSP-11A is the Array Processor System APS.

A few historical dates:
PRAKLA-SEISMOS' first mini processing system was the SSP-11 System, built around a fixed point convolver. The growing requirements for increased efficiency and floating point processing led to the development of an array processor and to the new system SSP-11A. At the beginning of 1975, the first array processor was ordered with the specifications drawn up by PRAKLA-SEISMOS. A universal array processor which fulfilled the modern seismic processing requirements was designed – the Array Processor System APS. In 1976, the APS prototype was installed at PRAKLA-SEISMOS and in the same year the first programs were running. Since 1977, the first SSP-11A with an integrated APS has been in operation.

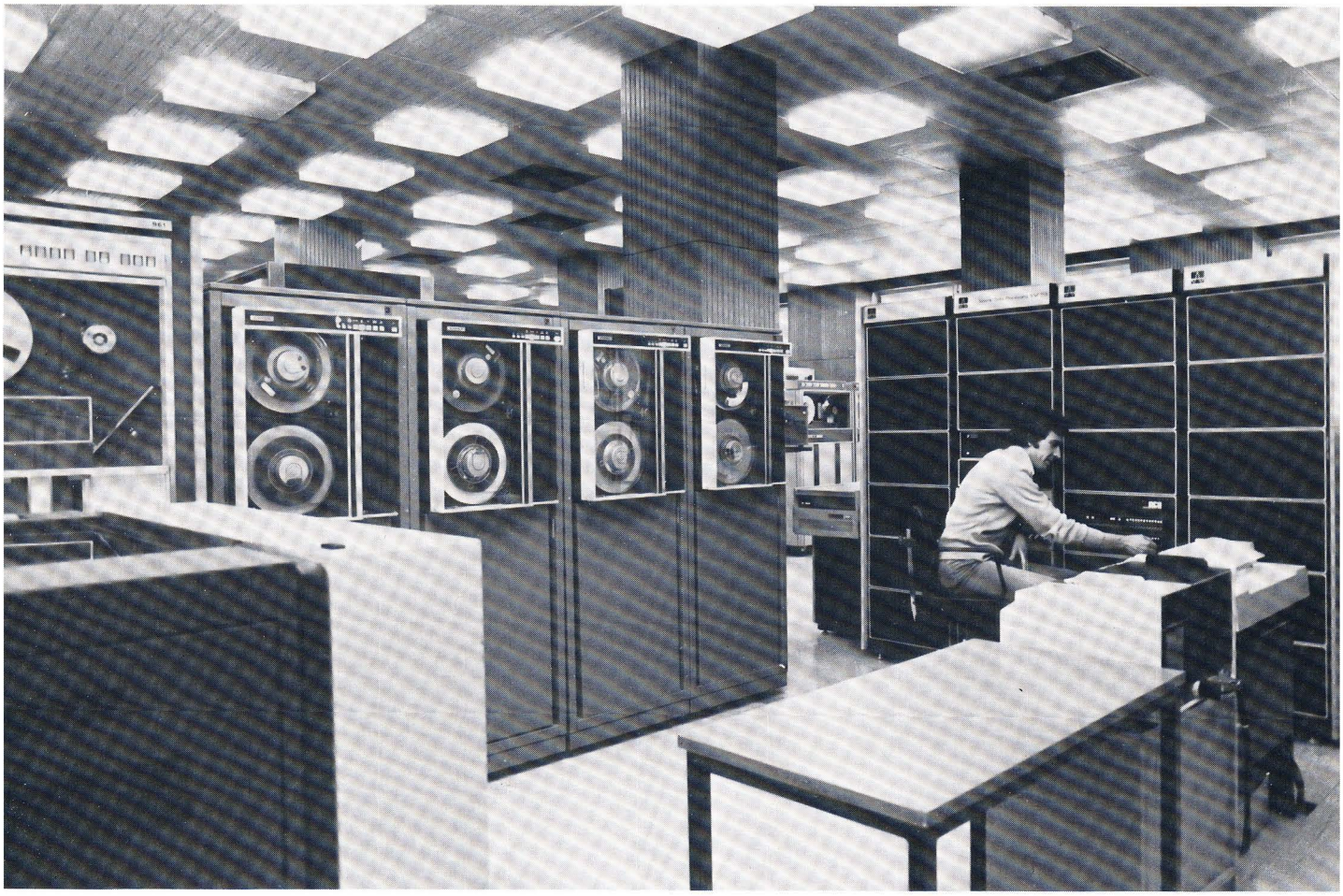
PRAKLA-SEISMOS' long experience in data processing was used in developing the APS. PRAKLA-SEISMOS, together with an efficient contractor for computer technology, designed a concept of which the most important features are

1. clear separation of work in distinct tasks to be carried out by specialized processors:
   - input/output of data by the Input/Output Processors
   - execution of arithmetic operations by the Floating Point Processor
   - system control and parallel operation control of all processors by the Bus Master.

2. modular structure, allowing the APS to be modified. The APS 2, APS 4 (in use at PRAKLA-SEISMOS at present), APS 8 and APS 16 are upward/downward compatible. Thus, an adaption to every requested performance is possible.
   For smaller execution times and lower performance requirements the series APM is available.

3. free programmable on an assembler level. The mnemotechnical expressions are similar to those for the host computer PDP 11, used in the SSP-11A System. Although the APS is a specialized computer, its free programming permits great flexibility. All future tasks can be as easily programmed for an APS as for a universal computer.

SSP-11A Seismic Data Processing System with integrated APS



APS Structure

Host Computer

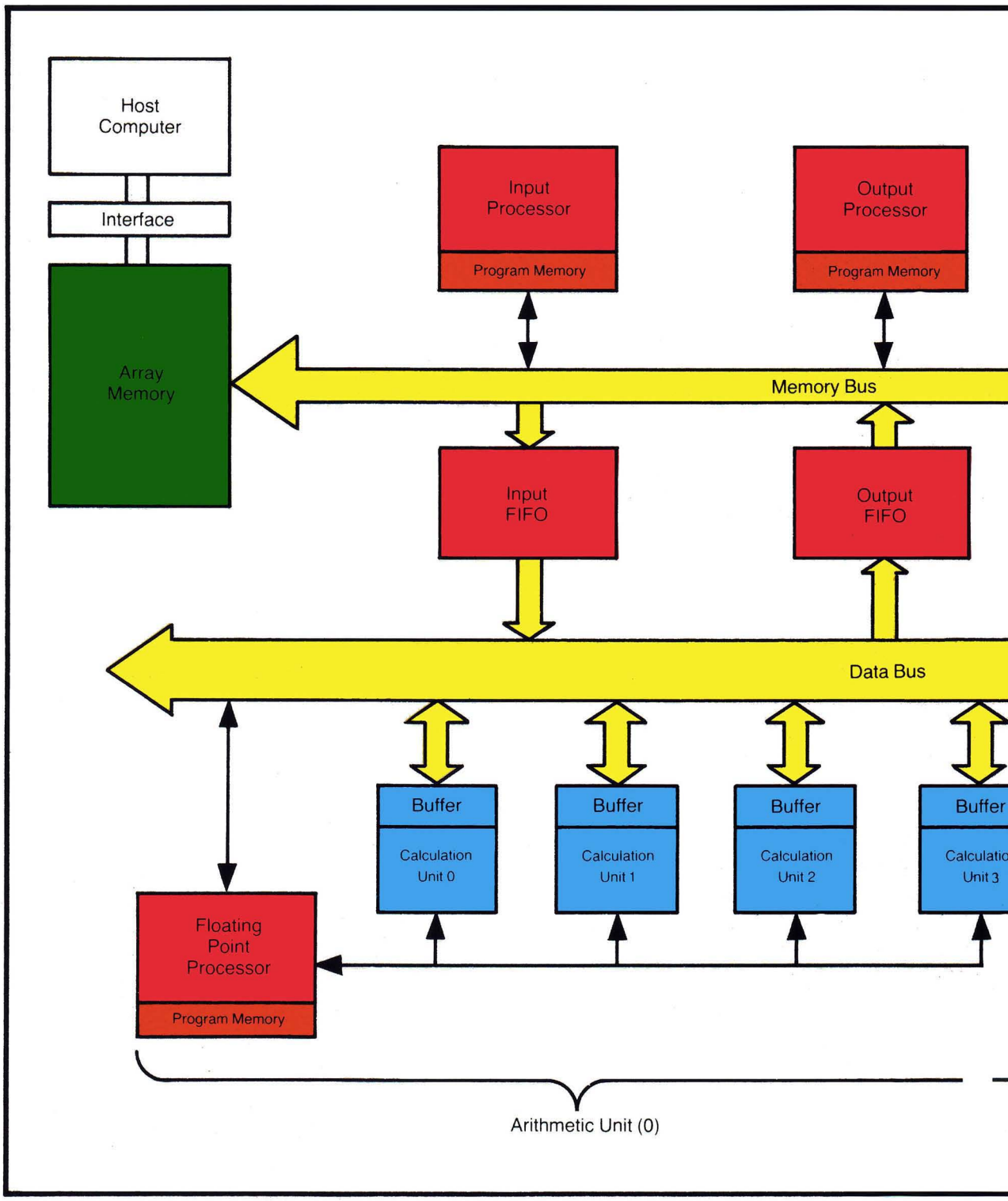
initializes APS and transfers data directly between its peripherals and the Array Memory

Input Processor

calculates addresses and transfers data from the Array Memory to the Input FIFO

Array Memory

is a data storage accessible from APS as well as from host computer



Floating Point Processor

controls the arithmetic and logical operations performed by the CUs

Calculation Units

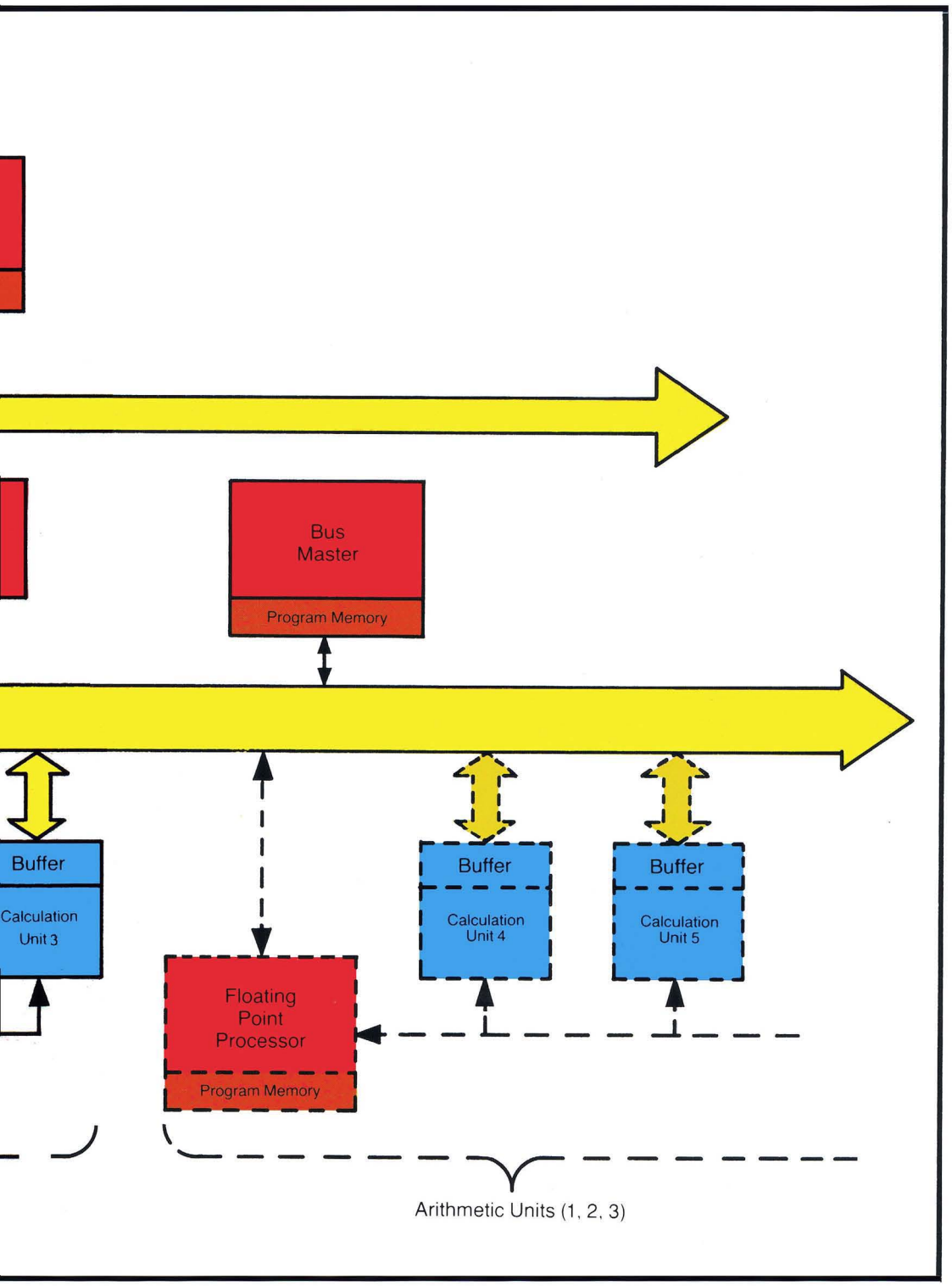
can process data with floating point and integer arithmetic, integer/floating point conversion and logical operations. Each CU consists of buffer, arithmetic unit and floating point accumulator. All calculation units work in parallel

Output Processor

carries out address calculations and transfers results from the Output FIFO to the Array Memory where they can be accessed from the host computer

FIFOs

ensure the transfer of data at maximum speed. They uncouple the APS-memory cycle times from the internal processing speed of the processors and calculation units, convert formats during data flow and prevent conditions such as overflow



Bus Master

has the function of a monitor: it controls the Data Bus and coordinates the operation of each processor and calculation unit

Data Bus and Memory Bus

are very fast buses allowing multiple transfer with only one bus cycle

Buffers

are 32 data registers for each calculation unit and can be accessed in different addressing modes. Paged and offset modes allow input, calculation, and output to occur simultaneously with automated synchronization

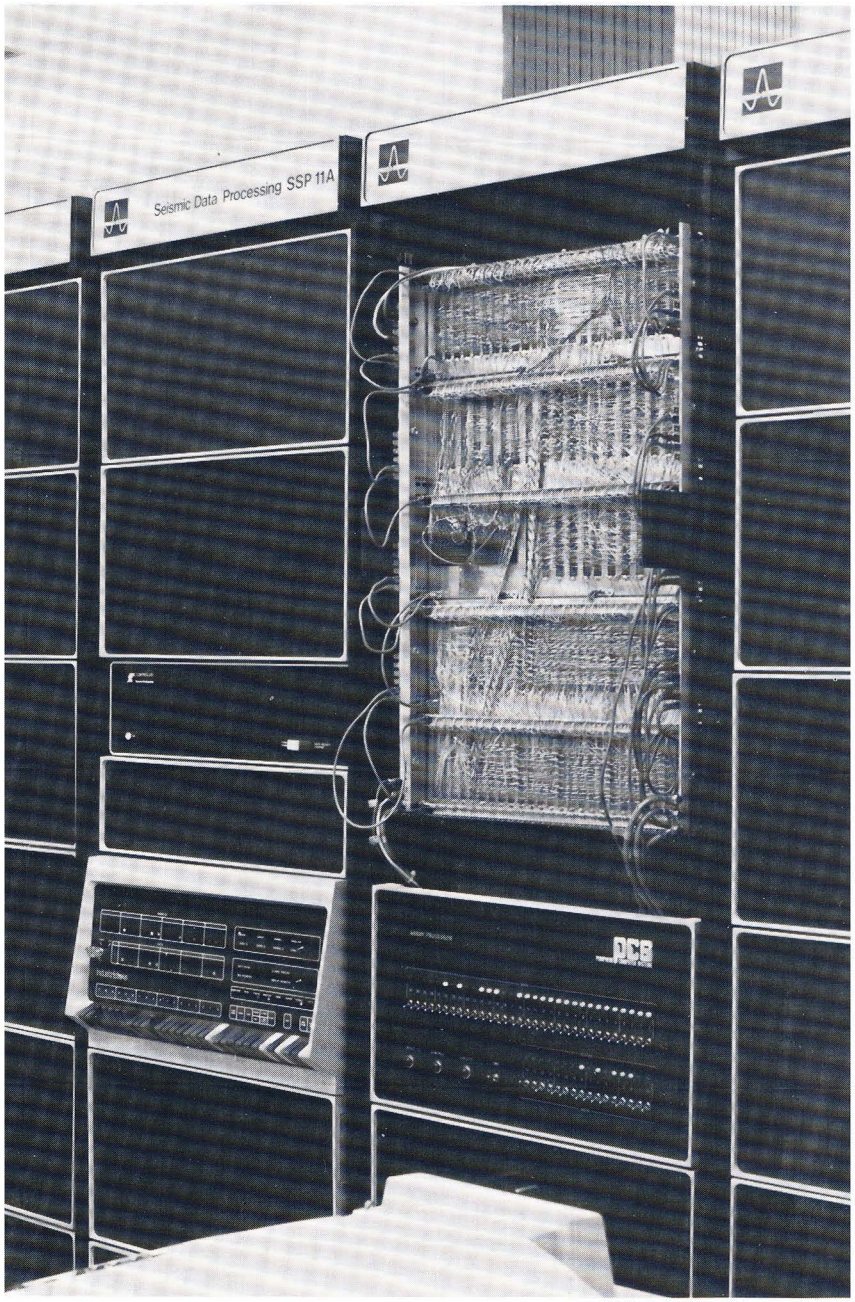
APS Operation

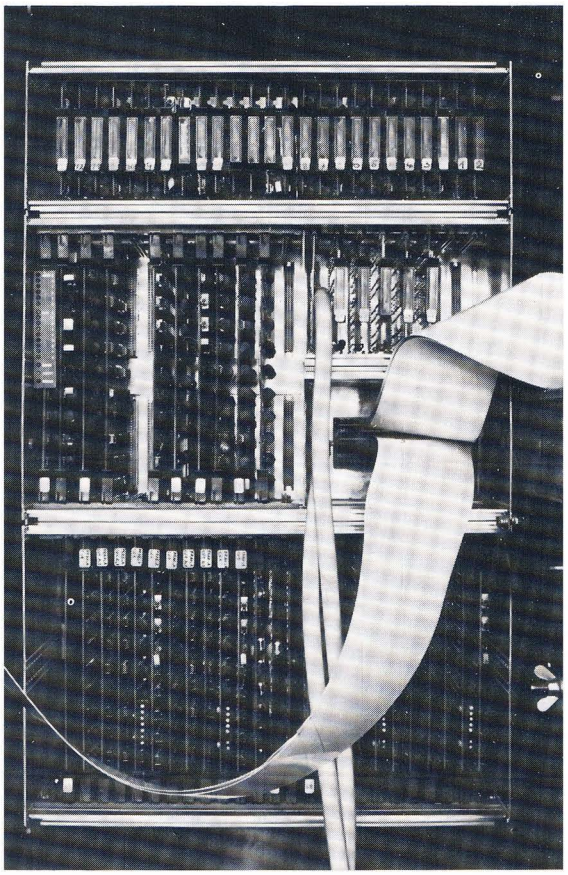
The order of the processors is shown on page 4/5. Each processor has its own specialized task and only needs to be programmed for its part of the process:

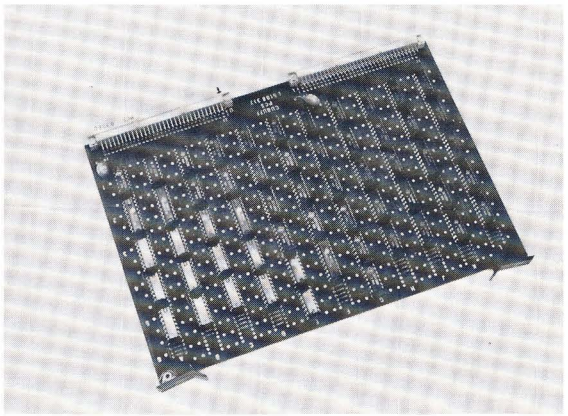
Data is input from the peripherals directly to the Array Memory by the host computer. The Input Processor can access the Array Memory and transfer data from any address calculated by the Input Processor to the Input FIFO. Data are queued in the Input FIFO until the Bus Master directs them to the Calculation Unit Buffers. There the data are processed under the control of the Floating Point Processor which also signals any error conditions such as overflow, underflow, etc. The results are transferred by the Bus Master to the Output FIFO where they are queued for transfer to the Array Memory by the Output Processor. Data can now be kept in the Array Memory for further processing or be output to peripherals by the host computer.

All processors and all calculation units work in parallel. The synchronization between processors and calculation units is hardware controlled; software control is also possible. When transferring data to or from the Calculation Unit Buffers, three addressing modes are available: direct addressing of the 32 Buffer words, paged mode, paged mode with offset; combinations of all three can also be chosen. Both paged modes utilize the hardware synchronization whereas paged mode with offset arranges data for filtering or similar processes and relieves the Input Processor of repetitious inputs.

Modern technology used in the APS







Technical Specifications

APS General

The parallel processors are of modular structure and allow expansion with the following possibilities:

Bus Master with
up to 2 Input Processors
up to 2 Output Processors
up to 4 Floating Point Processors

Parallel operations in 2, 4, 8 or 16 Calculation Units

Array Memory:

MOS
up to 128K 16-bit words
cycle time at overlapped operations: 200 ns
memory can be addressed byte-wise (PDP-compatible) and from Input/Output Processor either word-wise (16 bits) or double word-wise (32 bits)

Program Memory for Processors:

Bipolar
1K 16-bit words per processor
cycle time 100 ns

Bus cycle time:

180 ns

FIFOs:

Input FIFO: 6 x 36 bits (32 bits + 4 bits signal)
Output FIFO: 6 x 32 bits
IBM floating point format or host computer format conversion
to IBM on fly

CU Buffer:

32 x 32 bits buffer for each Calculation Unit

Bus Master:

4 Registers of 4 bits each

Input/Output Processor:

16 Registers of 16 bits each

Test Panel:

switches and indicators for 32-bit data
switches and indicators for 16-bit status

Standard electrical requirements:

220 V/50 Hz, 600 VA

Operating temperature range:

5 to 35 C

Mechanical mounting: APS is mounted in standard 19" (483 mm) cabinets
depth: 240 mm
height: 670 mm (APS 2, APS 4), 935 mm (APS 8), 1465 mm (APS 16)
weight: 36 kg (APS 4)

SSP-11A (APS 4)

In the SSP-11A System, PRAKLA-SEISMOS uses the APS 4 with the following configuration:

Bus Master with
1 Input Processor
1 Output Processor
1 Floating Point Processor

Parallel operations in 4 Calculation Units

Array Memory:

MOS
48K 16-bit words
cycle time at overlapped operations: 200 ns
memory can be addressed byte-wise (PDP-compatible) and from Input/Output Processor either word-wise (16 bits) or double word-wise (32 bits)

All other specifications are identical to those stated under »APS General«

Software

Complete software and documentation are available to meet the different needs of our customers:

The SSP-11A System is an optimal system for geophysical data processing utilizing the features of APS and the host computer PDP 11. This complete seismic system is designed for the customer who wants a reliable, ready-to-use system. It can easily be expanded by either using the library routines or by programming new modules as explained below.

The customer who wants to integrate the APS to other host computers than PDP will appreciate that FORTRAN-callable routines for vector and matrix operations, and signal processing functions are supplied with the APS.

The programmer will find the APS easy to program since each processor need only be programmed for its particular task. Programming is further facilitated by the symbolical language which has instruction sets for each processor specific to its task (see page 9). The parallel operation of all processors is mainly hardware controlled, this reduces or eliminates software synchronization.

APS Basic Software

Cross-assembler: assembles the processor source programs, determines and lists syntax errors and outputs a loadable segment.

Linker: Segments for the different processors are concatenated into one APS loadable program by the linker.

System handler: The on-line testing of APS-programs is enabled by the system handler. It allows the host to communicate with the APS-system for
loading and starting APS programs,
reading/writing data from/into APS Array Memory,
data and parameter transfer to processor memory,
status checking,
batch operations,
etc.

APP-Library: The APS Program Library contains routines for

- Vector operations for logic and arithmetic functions:
  scalar terms and conversions
  vector element sum, maximum or minimum
  vector clipping, limiting
- Vector operations for exponential and trigonometric functions:
  maximum and minimum magnitude
  peak
  two-vector maximum, minimum, magnitudes
- Matrix operation:
  inverse, transpose, multiply, vector multiply
- Signal processing functions:
  convolution
  FFT
  scrambling
  vector polynomial
  difference equation
  band pass filter
  recursive filter

Diagnostics: For preventive maintenance or trouble shooting either hard-wired APS tests can be started on-line or off-line, or extensive test programs can be loaded and started from the host computer. These tests check memory, buffers, FIFOs, all processor functions, data and signal transfer, communication and synchronization of all processors.

Instruction Set

The ambitious programmer can easily change or expand the existing functions and algorithms, or write new programs for system integration.

The instructions are in the most common and widely known 16-bit nomenclature. Each processor instruction set is particular to the task of the processor:

1. The main task of the Input/Output Processors is address calculation and data transfer. Both processors share 16 registers with 16 bits each and use one instruction set containing:

general instructions	MOV, CLR, TST, CMP, INV, NOP
arithmetic instructions	ADD, SUB, INC, DEC
bit operations	BIT, BIS, BIC
logical instructions	AND, OR, EOR
shifts	ASL, RSH, RASH
unconditional and conditional branches	BR, BEQ, BNE, BGT, BLE, . . .
data transfer between Array Memory and FIFOs, with or without format conversion between host and IBM format	LDR, LDD, LDS, STR, STD, STS
data transfer between Array Memory and processor registers	LD, STO
etc.	

2. The Bus Master instruction set contains the same general, arithmetic, logical, bit operations, and branch instructions as the Input/Output Processors, works with 4 registers, 4 bits each, and contains the additional control instructions:

enable/disable processors	ENA, DIS
load single status bits	LPF, LOP, LER, . . .
paging control instructions	PAG, SIZ, CIP, COP
bus transfers from source to destination (any processor, register or buffer can be either source or destination)	SS, DT
etc.	

3. The instructions of the Floating Point Processor are mainly arithmetic (floating point normalized and unnormalized or integer) for operations applied to the accumulator and/or buffers:

arithmetic instructions	FADD, FMUL, FDIV, . . . UADD, UMUL, UDIV, . . . ADD, SUB, . . .
conversion between floating point and integer	FFLT, IFX
unconditional and conditional branches	BR, BSE, BSN, . . .
etc.	

All Floating Point Processor instructions may furthermore be conditionally executed. For this purpose, there is a number of instructions for setting/clearing condition bits according to arithmetic results, e. g. zero, negative, positive, mantissa overflow, exponent underflow, divide error, etc.

Seismic Software

In the SSP-11A System, all time-consuming processes have been specifically programmed for the APS for greater efficiency. The following processes are available:

- Gain Recovery
- Normalizations
- Velocity Analyses
- Corrections
  - static and dynamic corrections
  - automatic residual static corrections
- Sortings (also for Areal Seismic)
- Stack incl. muting, ramping, weighting
- Filtering** (Time Variant)
- Deconvolution** (Time Variant)
  - spike
  - predictive
  - VIBROSEIS*
- Autocorrelation**, Crosscorrelation**
- Migrations
  - Kirchhoff summation
  - wave equation
  - and by Fourier Transform
- Power Spectra, Spectral Analyses
- VIBROSEIS* processing
- Real Amplitude Processing
- Continuous processing documentation on tape
- Contouring programs

** in frequency or time domain

* Trade Mark of Continental Oil Company

Execution Times

Array Processor System	APS-4	APS-8	APS-16
Hardware Commands 32-bit floating point			
Add/Subtract	125 ns	63 ns	32 ns
Multiply	250 ns	125 ns	68 ns
Divide	550 ns	275 ns	138 ns
Add/Subtract, integer	75 ns	38 ns	19 ns
Logic operation	75 ns	38 ns	19 ns
Format conversion, fixed/floating point	150 ns	75 ns	38 ns
Algorithms 32-bit floating point			
1024 x 32 pts Correlation	16,0 ms	8,0 ms	4,0 ms
1024 pts real FFT	5,4 ms	2,8 ms	1,5 ms
1024 pts complex FFT	9,8 ms	5,1 ms	2,7 ms

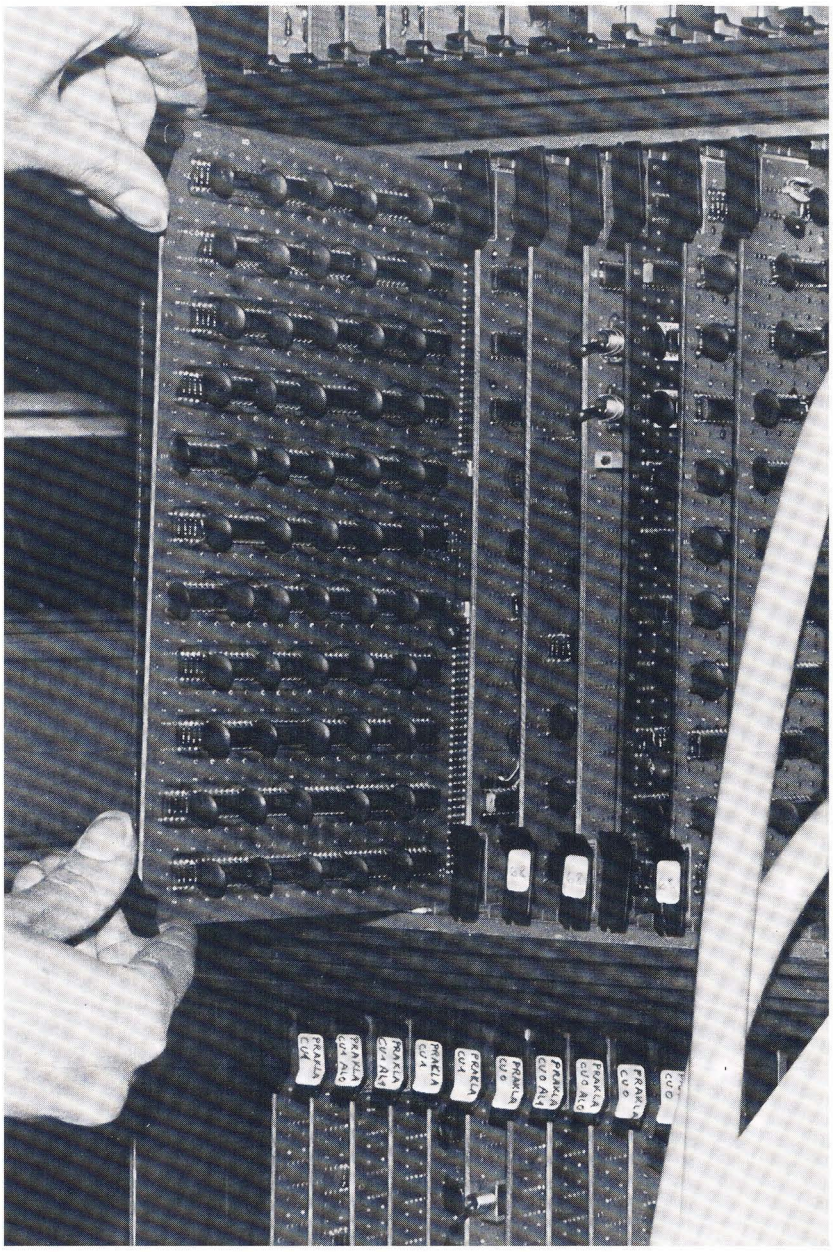
APS-8 and APS-16 include an additional Input Processor and Output Processor.

APS Operating System

The hard-wired operating system of the APS controls processor initialization, program loading of each processor, parameter transfer to/from Array Memory, and program execution. In addition, interrupts for special conditions such as errors are handled and passed on to the host computer.

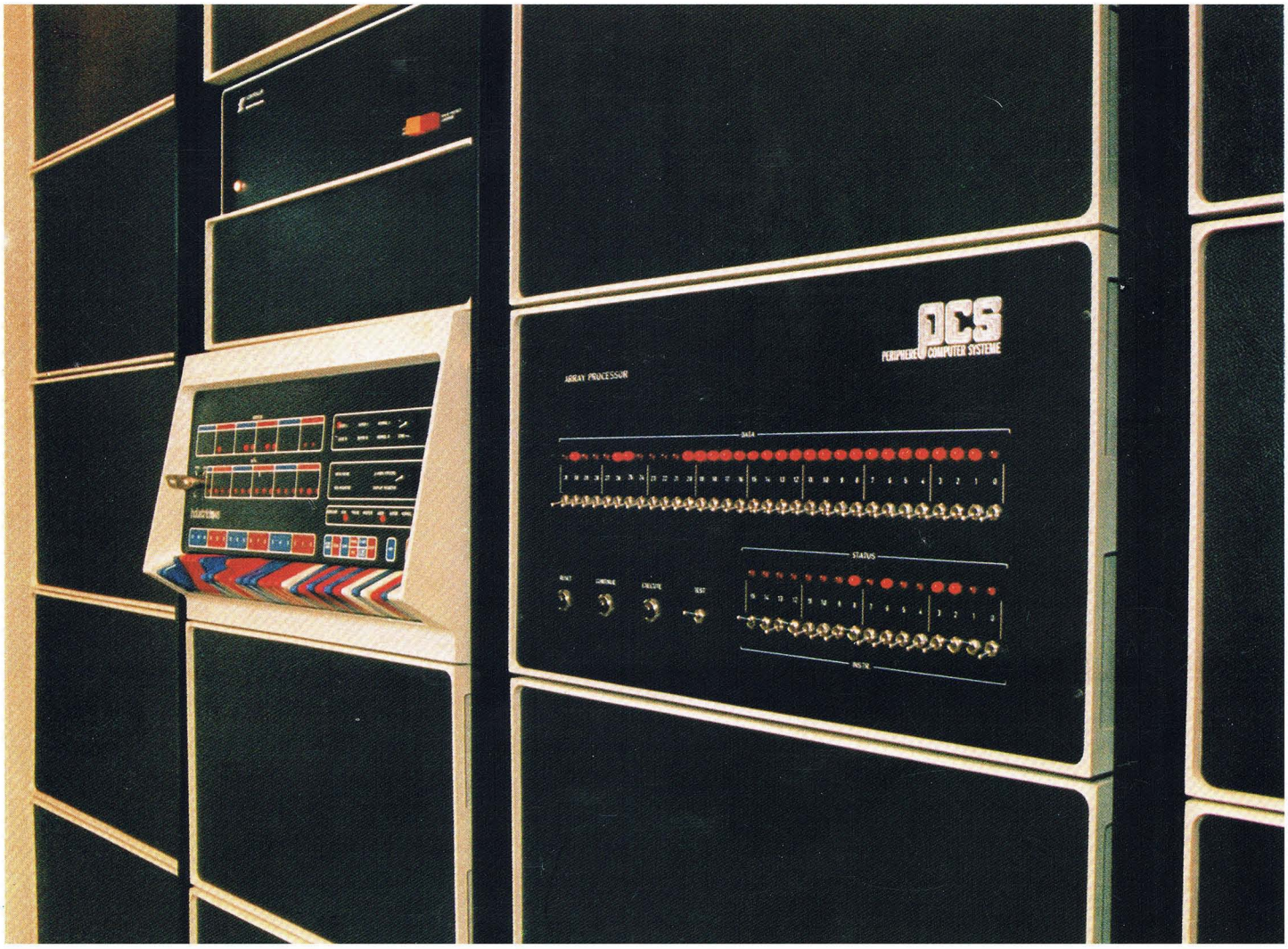
Modern Technology and High Reliability

For high speed, the APS uses Schottky-TTL logic: all boards are multi-wired providing high noise-immunity. Each APS is longtime tested in a climatic-chamber, thus ensuring high reliability. An extensive diagnostic package is supplied to facilitate maintenance.



Summary of the Most Important Features

- fast programmable multi-processor system
- arithmetic units for parallel calculation in floating point and integer, and logic operations
- modular structure, easy system expansion
- free programmable with widely known nomenclature
- standard data formats
- additional accumulator bits for optimal floating point precision
- interfacing for most minis as well as large scale computers
- fast data memory which can be integrated and used by the host
- fast processor program memory
- automatic overlapped operations of all processors
- test panel with switches and indicators for supervision, control access and tests
- complete software, operating system and documentation
- system responsibility for hardware, software and service



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